Dynamic Mapping of Intensive Embedded Applications in NoC-based Heterogeneous MPSoCs

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11/06/2014
Heterogeneous MPSoC Platforms for Embedded Systems

- Distinct features of different PEs can be exploited to achieve high performance
  - GPPs
  - DSPs
  - Graphics cores
  - FPGAs
  - ASIP

Ever increasing complexity of embedded applications demand for NoC-based MPSoC architectures for efficiency and scalability
Mapping
Mapping
Object Models

- Modeled as task graphs (Master-Slaves)
MPSoC architecture model
Run-time Mapping

Application Specifications (TGs)

H.263 decoder

JPEG decoder

MPEG4 decoder

Without Design Space Exploration (Without DSE)

With Design Space Exploration (DSE)

NoC-based Heterogeneous MPSoC Platform

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Run-time Mapping Alternatives (With DSE)

Application Specifications (TGs)

Design-time DSE (compute intensive analysis)

Allocate tasks to PEs

Current System Status

Run-Time Platform Manager

Allocating tasks to PEs

Mapping using DSE results

Mappings using different number of PEs

Application User demands

NoC-based Heterogeneous MPSoC Platform

General Purpose Processor

Reconfigurable Area

MPEG4 decoder

H.263 decoder

JPEG decoder

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Run-time Mapping Alternatives (Without DSE)

Application Specifications (TGs)

On the Fly Mapping (all the processing is performed at run-time)

Run-Time Platform Manager

Allocate tasks to PEs

NoC-based Heterogeneous MPSoC Platform

Current System Status

Without DSE

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Research Objectives

- Propose Dynamic mapping techniques for NoC-based Heterogeneous (GPPs+FPGAs) MPSoC platforms
- Optimize performance (execution time and energy consumption)
- Minimize the tasks mapping time
Major Contributions

- Simulator for Dynamic Embedded Applications Mapping in NoC-based MPSoCs
- Heuristics for Routing and Spiral Run-time Task Mapping in NoC-based Heterogeneous MPSoCs
- Heuristics For Dynamic Task and Communications Mapping In Noc-Based Heterogeneous MPSoCs
Simulator
Mapping Single-Task-per-Processing-Element

Heuristics for Routing and Spiral Run-time Task Mapping in NoC-based Heterogeneous MPSOCs
Existing Packing Strategy (Left, Down, Up, Right)
Static Routing
Dynamic Routing
Experimental Results

Execution Time comparison of proposed Approach with NN and BN respectively

Energy Consumption comparison of proposed approach with NN and BN respectively
Mapping Single-Task-per-Processing-Element

Heuristics for Dynamic Task and Communications Mapping in NoC-based Heterogeneous MPSocS
Manhattan packing strategy

(a) Left-Down-Up-Right packing strategy
(b) Manhattan packing strategy

Hardware Resources
Software Resources
Initial Task Placement
MORA Routing

XY Routing

MORA Routing
1) Energy Consumption Computation:

\[ EC_{Total} = \sum EC_w + \sum EC^{R}_{s_{ti}} + \sum EC^{s}_{ti} + \sum EC^{h}_{ti} \]

2) Execution Time Computation:

\[ T_{ti}^{exe} = T_{ti}^{upload} + T_{ti(s/h)}^{exe} + T_{map}^{ti} + T_{com\_master}^{ti} + T_{com\_map}^{master} + \sum_{n=1}^{slaves-number} \text{Max}T_{tn}^{exe} \]
Experimental Results

Applications generated by TGFF (3-4 Level, 1-3 Son)

Applications  (a) MWD, (b) VOPD, (c) PIP

An MPEG-4 Application
Heuristics for Dynamic Task and Communications Mapping in NoC-based Heterogeneous MPSoCs

Experimental Results

Flow for Running the Simulation
Heuristics for Dynamic Task and Communications Mapping in NoC-based Heterogeneous MPSoCs

Experimental Results

Execution Time comparison of PNN and PBN with MPNN and MPBN respectively when employing XY and MORA routing for three scenarios

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Experimental Results

Energy Consumption comparison of PNN and PBN with MPNN and MPBN respectively when employing XY and MORA routing for three scenarios.
Performance evaluation for large size applications

Execution Time of 10 applications for four application sets (Scenario 4), where each application contains 5, 10, 15 and 20 tasks
Experimental Results

Performance evaluation for large-size applications

Energy Consumption of 10 applications for four application sets (Scenario 4), where each application contains 5, 10, 15 and 20 tasks.
Experimental Results

**Complexity Comparison: Number of Searches**

Number of searches for all the tasks in different application sets for Scenario 4 when employing existing and Manhattan strategies.
Conclusions and Recommendations for Future Work
Conclusion

- Simulation tool
- Proposed novel packing-based techniques for run-time mapping of applications on MPSoC platforms for:
  - Single-task-per-PE
  - Multiple-tasks-per-PE (in progress)
- Packing-based approaches have been shown to outperform existing techniques
- Experimental results confirm that our proposed techniques achieves further improvements both in execution time and energy consumption
- Dynamic Mapping of communications can be a good solution to achieve high performance
Recommendations for Future Work

- Heuristics For Dynamic Multi-Tasks and Communications Mapping In Noc-Based Heterogeneous MPSoCs (In progress)
  - Uses values corresponding to real architectures.
  - Increasing Heterogeneity in Processing Elements
  - Realizing Run-time Mapping on FPGA-based Hardware Platforms
  - Migration and load balancing
  - Dynamic solver for clustering
Publications – Journals and Conferences


Thanks for your attention